



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Reg. No

Final Assessment Test(FAT) - Apr/May 2025

Programme	B.Tech.	Semester	Winter Semester 2024-25
Course Code	BEEE206L	Faculty Name	Prof. Kanimozhi G
Course Title	Digital Electronics	Slot	F1+TF1
		Class Nbr	CH2024250501386
Time	3 hours	Max. Marks	100

Instructions To Candidates

- Write only your registration number in the designated box on the question paper. Writing anything elsewhere on the question paper will be considered a violation.

Course Outcomes

- CO1: Develop digital logic circuits and apply to solve real world applications.
 CO2: Design and analyze digital circuits using Verilog HDL.
 CO3: Design and implement combinational circuits, sequential circuits and programmable logic devices.
 CO4: Analyze and synthesize complex digital modules and circuits for various applications.
 CO5: Able to identify and prevent various hazards and timing problems in a digital design.

Answer all Questions (10 × 10 Marks)

01. a) Simplify the given Boolean function, $F(A,B,C,D) = \sum (1, 4, 6, 12, 14)$ in SOP form using K-map. (5 marks)
 b) Consider the combinational circuit shown in Figure.1. Determine the truth table for the output, F as a function of four inputs. (5 marks)

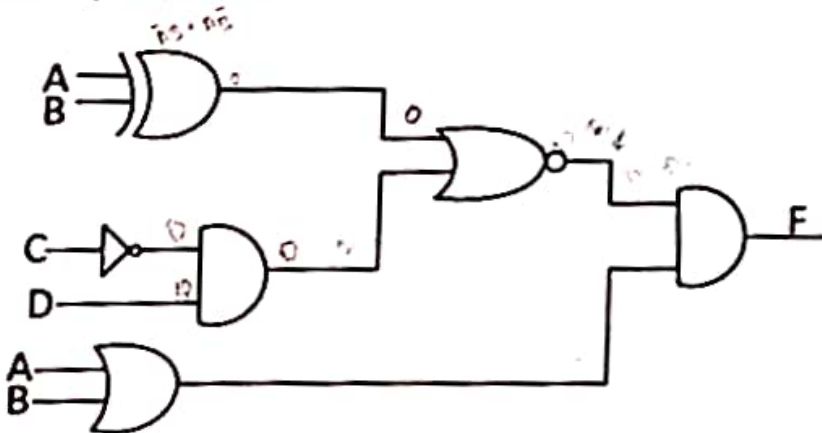


Figure.1

[10] (CO1/K2)

02. Determine a minimal SOP and POS expression for the following Boolean functions together with the don't care conditions d using four variable k map. Note that the don't care conditions have to be set to one value for the SOP solution and the other for the POS expression.

$$F(w,x,y,z) = \sum (1,9,10,11,12,13,14,15)$$

$$d(w,x,y,z) = \sum (3,5,8)$$

[10] (CO1/K2)

03. A certain logic circuit has four inputs A, B, C, and D. The output X of the circuit is logic 1, if two or more inputs are logic 1. Design an active low decoder.

- (a) Write truth table for this circuit. (3 marks)
 (b) Implement the function using one decoder with active low output. (3 marks)
 (c) Write Verilog code for the decoder. (4 marks)

[10] (CO2/K3)

04. Design an odd and even parity generator for a 4 bit string. Write Verilog code for 4 bit even parity generator.

[10] (CO3/K2)

05. For each set of binary numbers, determine the output states for the comparator of Figure.2 and implement a Verilog code for the 4-bit comparator.
- a) $A_3A_2A_1A_0=1100$ b) $A_3A_2A_1A_0=1000$ c) $A_3A_2A_1A_0=0100$
 $B_3B_2B_1B_0=1011$ $B_3B_2B_1B_0=1001$ $B_3B_2B_1B_0=0100$

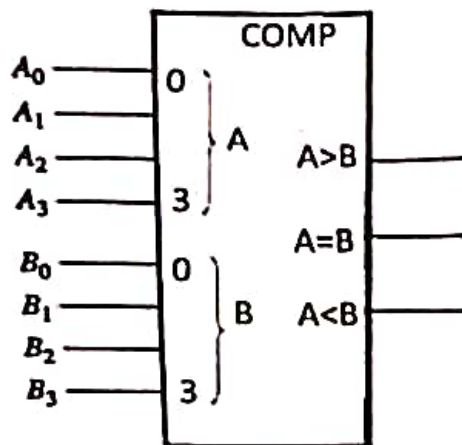


Figure.2

[10] (CO3/K3)

06. A sequential circuit has two JK flip flops, A and B; two inputs, x and y; and one output z. The flip flop input functions and the circuit output functions are as follows:

$$\begin{aligned} JA &= Bx + B'y' & KA &= B'xy' \\ JB &= A'x & KB &= A + xy' \\ Z &= Axy + Bxy' \end{aligned}$$

- (i) Draw the logic diagram of the circuit. (5 marks)
(ii) Tabulate the state table. (3 marks)
(iii) Derive the next state equations for A and B. (2 marks)

[10] (CO4/K4)

07. Design a synchronous counter which can count the random state sequence as 001, 100, 011, 101, 111, 110, 010, 001... using JK flip flops.

- a) Draw the state diagram. (2 marks)
b) Draw the state table and excitation table. (2 marks)
c) Draw the required K Maps and find the expression. (4 marks)
d) Draw the logic diagram of the given counter. (2 marks)

[10] (CO4/K4)

08. Explain Hazard free realization in digital circuits with examples.

[10] (CO5/K2)

09. Design a logic circuit with four inputs A, B, C, D that will produce output '1' only whenever two adjacent input variable are 1s. A and D are also treated as adjacent. Implement it using PAL.

[10] (CO4/K4)

10. Implement the following Boolean expression using Programmable Logic Array (PLA).

$$F_1(x, y, z) = \sum_m (1, 3, 4, 5, 7)$$

$$F_2(x, y, z) = \sum_m (1, 4, 5, 6)$$

[10] (CO4/K3)