Reg. No.:

Name :

VIT
CHENNAI
Vellore Institute of Technology

Continuous Assessment Test II – March 2024

Programme	:	**B. Tech. (CSE-AIM), B. Tech. (CSE), B. Tech. (CSE-CPS) & B. Tech. (CSE-AIR)**	Semester	:	**WS 2023-24**
			Code	:	**BECE102L**
Course	:	**DIGITAL SYSTEMS DESIGN**	Class Nbr.	:	**CH2023240502074, CH2023240502114, CH2023240502132, CH2023240502083, CH2023240502148, CH2023240502122, CH2023240502499, CH2023240503428, CH2023240502062, CH2023240502095**
Faculty	:	**Dr. Shoba S, Dr. Kiruthika V, Dr.Sukriti , Dr. Ranjeet Kumar, Dr. K. Srivatsan, Dr. Girija Shankar Sahoo, Dr. V.Sumathi, Dr. A. Bharathi Sankar, Dr. Ravi Tiwari, Dr. Dheeren Ku Mahapatra**	Slot	:	**A2+TA2**
Time	:	***90 Minutes***	Max. Marks	:	***50***

Answer ALL the questions

Q. No.	Sub. Sec.	Questions	Marks
1.	(i)	Construct the truth table of 4-bit parity generator for odd parity and implement its Boolean function using 4:1 multiplexer. [8 Marks]	8+7=15
	(ii)	Write a Verilog HDL program for designing 1 × 8 De-multiplexer using 1 × 2 De-multiplexer. [7 Marks]	
2.		Use a suitable algorithm, perform multiplication of **(14) x (-24).** **(i)** Find the register size used for the calculation using specific algorithm [1 mark] **(ii)** Elaborate each step of calculation using the algorithm selected, for the required number of steps or count. Show step wise algorithmic variables used, as a tabulation and obtain the final result [7 marks] **(iii)** Why you have selected the specific algorithm and mention any two advantages [2 marks]	10
3.		Design an adder circuit that reduces the propagation delay with inputs A= '1101' and B = '1000'. Explain the concept and determine the output for each stage. [7 Marks] Comment on the performance of the circuit compared to 4-bit parallel adder. [3 Marks]	10
4.	(i)	Build a holding circuit using data flip-flops, which creates a reel projector that displays the inputs on their respective output simultaneously until all the 5 pieces of inputs '11010' are filled. Design and write the Verilog HDL for the same. [8 Marks]	7+8=15
	(ii)	Imagine you are designing a security access control system for a high-security facility. The system requires a countdown timer that starts from 13 and decrements by one every second. When the countdown reaches 0, an alarm is triggered, indicating the end of a secure time window. Design a sequential circuit and sketch the timing diagram for the outputs.[7 Marks]	

Course Faculty

Reg. No.:	23BCE1608

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Continuous Assessment Test I – February 2024

Programme	:	**B.Tech (ECE/ECM)**	Semester	:	**WS 2023-24**
Course	:	**Digital Systems Design**	Code	:	**BECE102L**
			Class Nbr	:	CH2023240502145
Faculty	:	**Annis Fathima A**	Slot	:	**B1+TB1**
Time	:	**90 Minutes**	Max. Marks	:	**50**

General Instructions:

- Write only your registration number on the question paper in the box provided and do not write other information.
- Only non-programmable calculator without storage is permitted

Answer ALL the questions

Q.No.	Questions	Marks
1.	Sketch the combinational logic circuit diagram for the design of a "Fire alert system" based on abnormalities detected by a flame sensor (F), smoke sensor (S) and a temperature sensor (T). The alarm (A) will be activated only when 2 or more sensors detect abnormalities. Include associated truth table, K-map and minimum literal Boolean expression. Also, sketch the NOR only representation of the circuit.	3+2+2+3
2.	Design the CMOS Logic circuit for the expression F= (A + (B' + CD)')'.	10

3.	Find the value of a,b,c,d from the given code at the mentioned timings.
	module q3;
	reg a,b,c,d;
	
	initial
	begin
	a=1'b0;
	b=1'b1;
	c=1'b0;
	#10 b=1'b0;
	#5 a=1'b1;
	end
	
	initial
	begin
	#5 d= (a|c);
	#15 d= (b|c);
	#20 d=(b|c);
	end
	endmodule
		10

Time (ns)	a	b	c	d
0	0	1	0	
5	0	1	0	0
10	0	0	0	
15	1	0	0	
20				b|c
30				
40				b|c

4. Find the errors in the given Verilog HDL code. **10**

```
1  module gen  cal (a,b,c)
2  input a,B;
3  output c:
4  Wire c1;
5  assign c1 == c;
6  always @ (a or b);
7  begin
8  assign c1 = a%b;
9  end;
10 always @ {a or b}
11 begin
12 #10 c1 <= 2'b01;
13 End
14 end module;
```

5. A student wants to make a circuit which will route the digital information from each of the 4 data inputs to the output Y based on the 2 control inputs. Name the circuit which the student wants to implement. Illustrate how the binary data needs to be given to control inputs for routing the data from each data input to the single output Y with truth table. Construct the required logic circuit using NAND only logic. **2+4+4**

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Reg. No.: 23BPS1166

Name :

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Continuous Assessment Test I – January 2024

Programme	:	B. Tech (CSE=AIM), B. Tech(CSE), B. Tech(CSE-CPS) & B. Tech(CSE-AIR)	Semester	:	WS 2023-24
			Code	:	BECE102L
Course	:	DIGITAL SYSTEM DESIGN	Class Nbr	:	CH2023240502074, CH2023240502114, CH2023240502132, CH2023240502083, CH2023240502148, CH2023240502122, CH2023240502499, CH2023240503428, CH2023240502062
Faculty	:	Dr. Shoba S, Dr. Kiruthika V, Dr.Sukriti , ,Dr.Ranjeet Kumar, Dr.K. Srivatsan, Dr.Girija Shankar Sahoo, Dr.V.Sumathi, Dr. A. Bharathi Sankar, Dr Ravi Tiwari	Slot	:	A2+TA2
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		(i) Simplify the following function using Boolean Algebra and express using canonical POS F(A,B,C,D) = (D' + AB' + A'C + AC'D + A'C'D)' (ii) Express the following function using canonical POS F(A,B, C) = AB + (AC)' + AB'C(AB+C)	[5+5]
2.		Simplify the following function using K- Map F(A, B, C, D) = π (3, 4, 5, 6, 7, 10, 11, 14, 15). Also, Implement the obtained function using NOR gates only.	10
3.		Implement the following Boolean function using CMOS logic $OUT = \overline{D + A \cdot (B + C)}$	5
4.		Simplify the following Boolean function F1=∑ (1,2,3,6,8,9,10,12,13,14) and Write the Verilog program using (a) Behavioral and (b) Dataflow modelling.	10
5.		Implement a full adder using n:2^n combinational circuit	8
6.		Find all the errors (syntax and logical) in the following Verilog declarations. *module Exmpl-3(A, B, C, D, F)* // Line 1 *inputs A, b, C, Output D, F,* // Line 2 *output B;* // Line 3	7

```
and (A, B, D);          // Line 4
and g1(y,A,B);          // Line 5
not g2(D, A, C);        // Line 6
OR (F, B; C);           // Line 7
    endmodule;          // Line 8
```

Course Faculty

Reg. No.: 23BAI1038

Name : Adithiyaa.D

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Continuous Assessment Test I – February 2024

Programme	: B.Tech. (CSE – All Programme)	Semester	:	WS 2023-24
Course	: Digital System Design	Code	:	BECE102L
		Slot	:	A1 + TA1
Faculty	: Dr. RANJEET KUMAR Dr. G LAKSHMI PRIYA Dr. DHEEREN KU MAHAPATRA Dr. KIRUTHIKA Dr. GIRIJA SHANKAR Dr. SUKRITI Dr. JEAN JENIFER NESAM J	Class Nbr	:	CH2023240502023 CH2023240502025 CH2023240502027 CH2023240502029 CH2023240502033 CH2023240502045 CH2023240502054
Time	: 90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Questions	Marks
1.	Simplify the following function using K-map, F=ABCD+AB'C'D'+AB'C+AB. Realize the simplified expression as (i) SOP using only NAND gates (ii) POS using only NOR gates	15
2.	Implement the following Boolean expression using CMOS logic style; Z = [(D + E + A)(B + C)]'	5
3.	Design a combinational circuit with four inputs (A, B, C, and D) such that the output (Z) is 1 if the binary representation of the inputs contains more 1's than 0's. Implement the Boolean expression for this condition using logic gates and provide a structural Verilog code for the resulting circuit.	10
4.	Create a digital system with 'M (=2^N)' inputs to 'N' outputs, where 'N = 3,' using coded binary representation. Implement the system in Verilog using behavioral modeling and provide a corresponding test bench.	10

5.	Rewrite the following Verilog code without any errors.
	Module 42code(d,y0,y1);
	input [3:0]d;
	output Y0,y1;
	always @(d)
	begin
	out0 = d[0] & d[1];
	out1 = d[2] | d[3]
	end
	end module
		5

6.	Implement the following Boolean expressions using half adders. D= A ⊕B ⊕C E= (A ⊕B) C	5

Reg. No.: 23BAI1038

Name : Adithyaa.D

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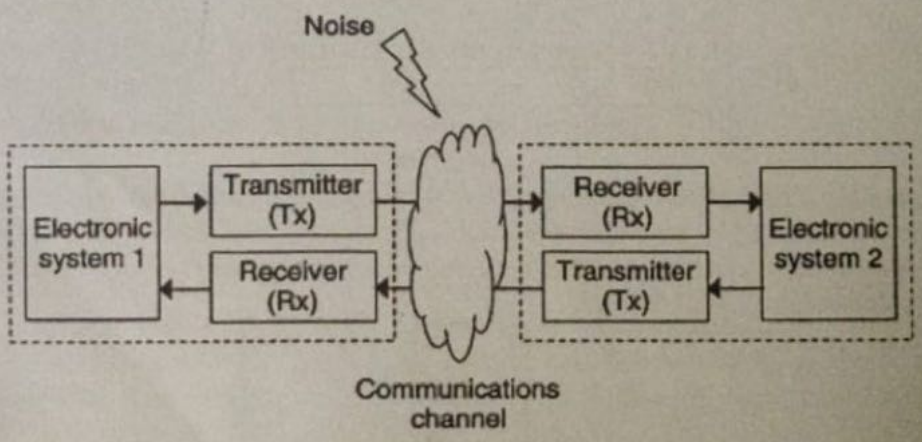
Continuous Assessment Test II – March 2024

Programme	: B.Tech. (CSE – All Programme)	Semester	:	WS 2023-24
Course	: Digital System Design	Code	:	BECE102L
		Slot	:	A1 + TA1
Faculty	: RANJEET KUMAR	Class Nbr	:	CH2023240502023
	G LAKSHMI PRIYA			CH2023240502025
	DHEEREN KU MAHAPATRA			CH2023240502027
	KIRUTHIKA			CH2023240502029
	GIRIJA SHANKAR			CH2023240502033
	SUKRITI			CH2023240502045
	JEAN JENIFER NESAM J			CH2023240502054
Time	: 90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		 **Figure.1** Errors may arise during the data transmission process depicted in Figure 1 when noise is introduced into the signal. These errors occur particularly when the level of noise surpasses a threshold significant enough to disrupt the transmitted data. To ensure data transmissions between communication nodes are accurate, design an even parity checker with data inputs A, B, and C. Also implement the circuit using suitable multiplexer and write the Verilog HDL code for the same.	10
2.		Identify and implement the algorithm that involves 2's complement, addition, subtraction and shifting operations, to perform multiplication of two numbers 15 and -12. Elaborate on the step-by-step procedure involved using a flowchart.	10
3.		(a)Can JK flip-flop be considered as a universal flip-flop? If yes, then justify by comparing and contrasting with the help of its truth table and other flip-flops. (6 marks)	10

(b) Complete the timing diagram shown in Figure 2 for two types of D flip-flop devices: (i) an active HIGH enabled latch and (ii) a positive edge-triggered D flip-flop. (4 marks)

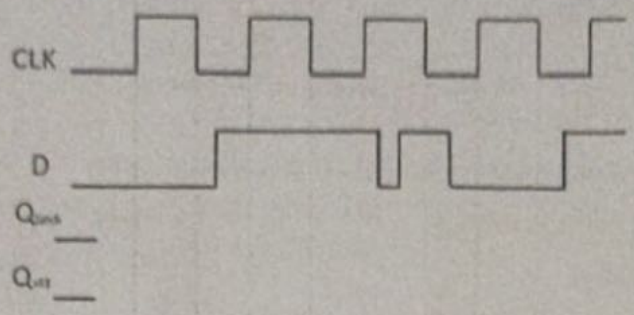


Figure.2

4. Consider a control unit for a wheat packing machine to pack wheat of 6kg each. Present weight of the pack is measured and then it is compared with the reference value (6kg). If the wheat pack is less/greater than 6kg control signal generated to add/remove excess wheat into/from the wheat pack. If the wheat pack weight is exactly 6kg then control signal is generated to make a pack. Design an appropriate control circuit for the above mentioned comparison operation using basic logic gates. Also write a Verilog HDL code in dataflow modelling for the same. 10

5. (a) Draw the logic diagram of a 4-bit register incorporating D flip-flop and a 4 × 1 multiplexer with mode selection inputs S_1 and S_0. The register functions according to the following Table 1: (5 Marks) 10

S_1	S_0	Register Operation
0	0	No change
0	1	Complement the output
1	0	Clear register to 0
1	1	Load Data

Table. 1

(b) For the circuit shown in figure 3, two 4-bit parallel-in serial-out shift registers loaded with the data shown are used to feed the data to a Full Subtractor (FS). Initially, all the flip-flops are in clear state. After applying two clock pulses, identify the outputs of the Full Subtractor (FS). (5 Marks)

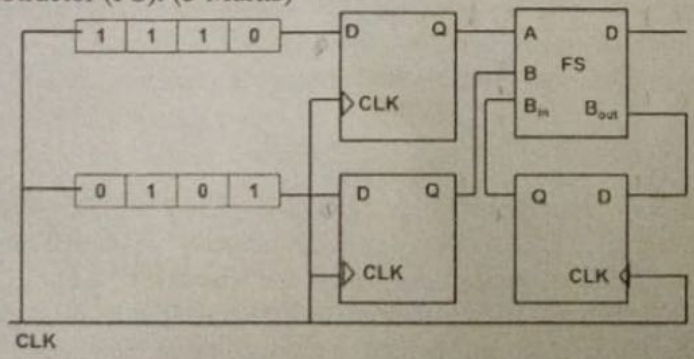


Figure.3