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Vellore Institute of Technology
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CHENNAI

Reg No

Final Assessment Test(FAT) - Apr/May 2025

Programme	B.Tech.	Semester	Winter Semester 2024-25
Course Code	BECE102L	Faculty Name	Prof. Idayachandran G
Course Title	Digital Systems Design	Slot	C1+TC1
		Class Nbr	CH2024250502908
Time	3 hours	Max. Marks	100

Instructions To Candidates

- Write only your registration number in the designated box on the question paper. Writing anything elsewhere on the question paper will be considered a violation.

Course Outcomes

CO1: Optimize the logic functions using and Boolean principles and K-map
CO2: Model the Combinational and Sequential logic circuits using Verilog HDL
CO3: Design the various combinational logic circuits and data path circuits
CO4: Analyze and apply the design aspects of sequential logic circuits
CO5: Analyze and apply the design aspects of Finite state machines
CO6: Examine the basic architectures of programmable logic devices

Section - I
Answer all Questions (4 × 10 Marks)

01. (a) Consider a = 4'b1010 and b= 4'b0101 and find the output of each line of the Verilog code given below. Each line is executed independently. (5 marks)

```
u = (a > b) ? a : b;
v= (a > b) && (b > 2);
p = (a & !b);
q = (a < b) || (b == 5);
r= !(a == b);
```

(b) From the testbench module given below, draw the timing waveforms for clk, reset and preset (5 marks)

```
module waveform_tb;
 reg clk, reset, preset;

 initial clk = 0;
 always #5 clk = ~clk;

  initial begin
   reset = 1;
  #10 reset = 0;
  #10 reset = 1;
   #15 reset = 0;
end

 initial begin
   preset = 0;
#15 preset = 1;
#10 preset = 0;
#10 preset = 1;
 end
endmodule
```

[10] (CO2/K3)

02. (a) Consider designing a frequency divider circuit for a digital clock with a T Flip-Flop to toggle the clock signal efficiently. However, only SR Flip-Flops are available in stock. Design a logic circuit to convert the SR Flip-Flop into a T Flip-Flop and show the step by step procedure involved in the conversion process. (5 marks)
(b) The shift register shown in Fig. 1 is initially loaded with the bit pattern 1111 (Q3Q2Q1Q0). Subsequently, the shift register is clocked, and with each clock pulse the pattern gets shifted by one-bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). Provide the sequence of outputs (Q3Q2Q1Q0) produced by the shift register for the next 5 clock pulses.(5 marks)

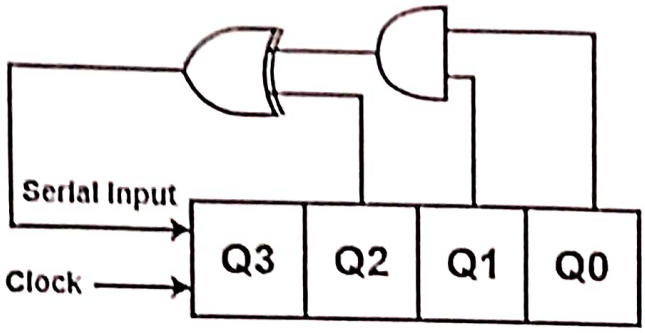

Fig. 1

[10] (CO4/K3)

03. Write a Verilog code using behavioral modelling for 8 bit ALU. The circuit has two inputs A and B, one output Y and three bit select bus. ALU also has an active low enable line. ALU performs arithmetic and logical operation as given below in the Table 1.

Table 1

Sel	Operation
000	Y= Bitwise complement of A
001	y= Logical complement of B
010	Y=A bitwise OR with B
011	Y=A logical AND with B
100	Y=A+B
101	Y=A-B
110	Y=A XOR B
111	Y=8'bFF

[10] (CO3/K3)

04. Consider designing a smart elevator control system that must prevent overcrowding by ensuring a maximum of 4 people can enter. The system uses an Infrared light sensor pair (IR Tx/Rx) at the elevator entrance to detect each person entering/exiting. Design an appropriate synchronous up/down counter using D flip-flops that increment by 1 when someone enters and decrement by 1 when someone exits.

[10] (CO4/K3)

Section - II
Answer all Questions (4 × 15 Marks)

05. Simplify the given Boolean function and design its corresponding logic circuit.
$F(A,B,C,D) = \sum m(1,3,4,6,8,9,11,13,15) + \sum d(0,2,14)$
Implement the final logic circuit using only NAND gates and CMOS logic. Compare the implementation with the original logic circuit and conclude the necessity of using NAND logic and CMOS logic in digital design

[15] (CO1/K3)

06. (a) Implement the given Boolean expression using a 4×1 multiplexer, considering a and b as select lines. (8 marks)
$F(a,b,c,d) = \sum m(1,13,14)$

(b) Convert the given function into SOP and Implement the obtained function using a 3×8 decoder. (7 marks)
$F(a,b,c,d) = \prod M(2,7,11,12)$

[15] (CO3/K3)

07. The state diagram of a sequence detector is given below in Fig. 2. State S_0 is the initial state.
(i) Identify the model, and find the sequence. (5 marks)
ii) Construct the state transition table (5 marks)
iii) Construct state equations and build the logic diagram using D-FF (5 marks)

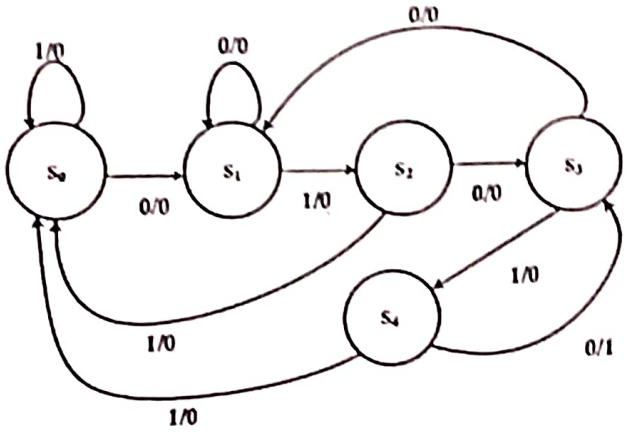

Fig. 2 **[15] (CO5/K3)**

08. (a) Design and implement the given function using a logic circuit with programmable AND gates and a fixed OR gate array. Explain how this structured approach helps in simplifying circuit design and discuss its advantages over traditional fixed-logic implementations. (10 Marks)

$F_1(x, y, z) = \sum m(1, 2, 4, 6)$
$F_2(x, y, z) = \sum m(0, 1, 6, 7)$
$F_3(x, y, z) = \sum m(2, 6)$
$F_4(x, y, z) = \sum m(1, 2, 3, 5, 7)$

(b) Compare the difference between CPLD and FPGA in terms of complexity and functionality (5 Marks)
[15] (CO6/K3)

BL-Bloom's Taxonomy Levels - (K1-Remembering,K2-Understanding,K3-Applying,K4-Analysing,K5-Evaluating,K6-Creating)