VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

CHENNAI

24BRS1046

Final Assessment Test(FAT) - Apr/May 2025

Programme	B.Tech.	Semester	Winter Semester 2024-25
Course Code	BECE102L	Faculty Name	Prof. Subhashini N
Course Title	Digital Systems Design	Slot	A1+TA1
		Class Nbr	CH2024250501667
Time	3 hours	Max. Marks	100

Instructions To Candidates

- Write only your registration number in the designated box on the question paper. Writing anything elsewhere on the question paper will be considered a violation.

Course Outcomes

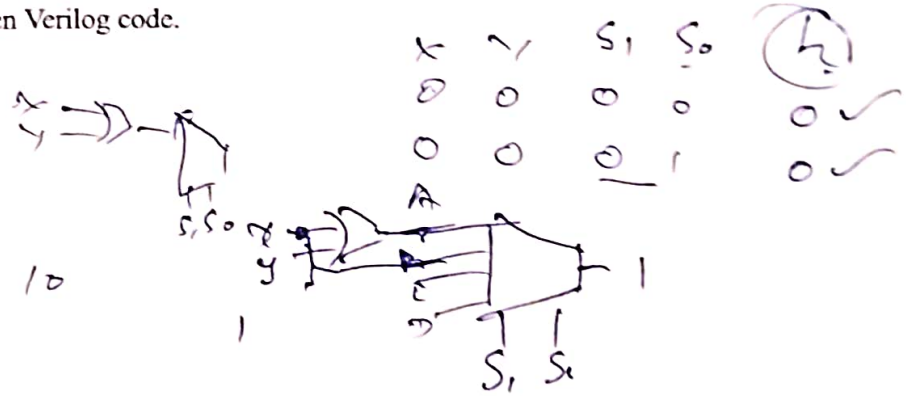
CO1: Optimize the logic functions using and Boolean principles and K-map
CO2: Model the Combinational and Sequential logic circuits using Verilog HDL
CO3: Design the various combinational logic circuits and data path circuits
CO4: Analyze and apply the design aspects of sequential logic circuits
CO5: Analyze and apply the design aspects of Finite state machines
CO6: Examine the basic architectures of programmable logic devices

Section - I

Answer all Questions (3 × 10 Marks)

01. Draw the digital logic circuit for the given Verilog code.

```
module logic_level(x, y, s, h);
input x, y;
input [1:0] s;
output reg h;
always @ (x, y, s)
begin
   case (s)
      2'b00: h = x | y;
      2'b01: h = x;
      2'b10: h = ~x & y;
      2'b11: h = y;
   endcase
end
endmodule
```



[10] (CO2/K2)

02. A digital system requires a combinational circuit capable of performing both binary addition and subtraction of two 4-bit numbers. The system should efficiently handle both operations using a minimal hardware. (Each 5 Marks)

a) Propose a circuit design that meets the given requirement.

b) Explain how the circuit differentiates between addition and subtraction without using separate units.

[10] (CO3/K3)

03. Implement the following function using a PLA :

$$Y_0 = \bar{A}\,\bar{B} + AB + B$$

$$Y_1 = \bar{A}\,\bar{B} + \bar{A}B + A\bar{B}$$

$$Y_2 = \bar{A}\,\bar{B} + \bar{A} + B + A\bar{B}$$

[10] (CO6/K3)

Section - II
Answer all Questions (2 × 15 Marks)

04 For the logic circuit shown in fig. 1,

(a) Write the minterms for the output function F and obtain the POS form of the output function F. (5 marks)

(b) Draw the logic circuit for the function obtained in (a) using NOR gates only. (5 marks)

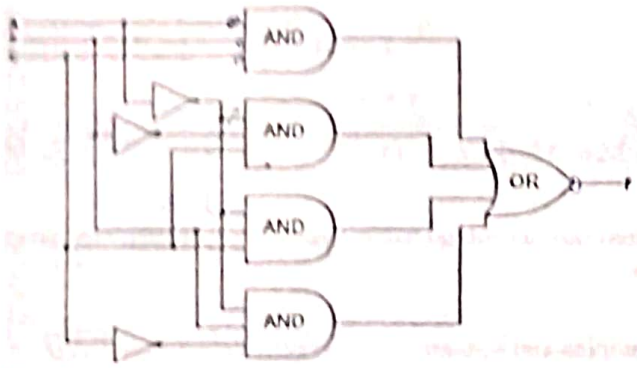


Fig. 1

(ii) Draw the CMOS logic circuit for the Boolean expression given below. (5 marks)

$$Y = \overline{(ABC + DE + F)}$$

[15] (CO1/K2)

05. Design a Moore sequence detector (1 bit Overlapping) to detect a sequence 1110 using D filpflop.

[15] (CO5/K2)

Section - III
Answer all Questions (2 × 20 Marks)

06. (i) A factory has several safety sensors labeled D0 to D7, each associated with different types of hazards. Each sensor, when activated, indicates a specific safety concern, with higher-numbered sensors having priority over lower-numbered ones due to their severity. A control system encodes the highest-priority hazard currently detected into a binary signal sent to a central monitoring station. Additionally, the system produces an output signal V, indicating whether any hazard is currently detected.

(a) Identify the digital circuit and provide the truth table showing how the active sensor inputs (D0 to D7) are encoded into the binary output signals and the hazard-detection indicator V. (6 marks)

(b) Determine the binary signal sent to the central monitoring station when both sensor D2 and sensor D6 are activated simultaneously. (2 marks)

(c) Determine the value of the hazard-detection signal V under the same condition, and explain what this value indicates about the system's status. (2 marks)

(ii) Design a 16 × 1 multiplexer with only 4 × 1 multiplexers, and write the Verilog code for the complete implementation. (10 marks)

[20] (CO3/K3)

07. (i) Design a system to monitor cars entering a small parking lot with space for 6 cars. A sensor detects each car entering and increases the count using a counter. When the count reaches 6, the entrance gate should automatically close and the counter gets reset. Create a ripple counter for this system and draw a timing diagram showing how the count changes. (15 marks)

(ii) A barcode scanner system is used in a supermarket to read product codes and send the data to a central processing unit. The scanner captures one bit of data per clock cycle and stores the entire 4-bit product code before passing it to the billing system. To implement this, design a shift register and write the Verilog code of the designed circuit. (5 marks)

[20] (CO4/K3)

BL-Bloom's Taxonomy Levels - (K1-Remembering,K2-Understanding,K3-Applying,K4-Analysing,K5-Evaluating,K6-Creating)