VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

24BLC1198

Final Assessment Test(FAT) - Apr/May 2025

Programme	B.Tech.	Semester	**Winter Semester 2024-25**
Course Code	BECE102L	Faculty Name	**Prof. Idayachandran G**
Course Title	Digital Systems Design	Slot	**C2+TC2**
		Class Nbr	**CH2024250502911**
Time	3 hours	Max. Marks	**100**

Instructions To Candidates

- Write only your registration number in the designated box on the question paper. Writing anything elsewhere on the question paper will be considered a violation.

Course Outcomes

CO1: Optimize the logic functions using and Boolean principles and K-map
CO2: Model the Combinational and Sequential logic circuits using Verilog HDL
CO3: Design the various combinational logic circuits and data path circuits
CO4: Analyze and apply the design aspects of sequential logic circuits
CO5: Analyze and apply the design aspects of Finite state machines
CO6: Examine the basic architectures of programmable logic devices

Section - I
Answer all Questions (4 × 5 Marks)

01. For the initial block statement given below, find the value of a,b,c,d, and e at the timestamps of 0,10,15,40, and 45

```
initial
begin
a = 1'b0;
b = #10  1'b1;
c = #5  1'b0;
d = #25  {a, b, c};
e = #5  |d;
end
```

[5] (CO2/K3)

02. If A = 1'b1; B = 2'b00; C = 2'b10; D = 3'b110; E = 3'b111, find the value of Y for the Verilog HDL code given below after executing each line. Each line is executed independently.

(i) Y = {{4{A}},{2{B}},C,D};
(ii) Y = D << 2;
(iii) Y = D|E;
(iv) Y = D||E;
(v) Y = (|D)+(|E);

[5] (CO2/K3)

03. Realize SR flip-flop using JK flip-flop. Show the conversion table and draw the circuit diagram.

[5] (CO4/K2)

04. Write a Verilog code that implements a 4-bit Johnson counter.

[5] (CO4/K3)

Section - II
Answer all Questions (2 × 10 Marks)

05. Derive and implement the logic expressions for Carry Generate (G) and Carry Propagate (P) for a 4-bit Carry Look-Ahead Adder (CLA) with necessary architectural diagrams. Based on your analysis, explain why Ripple Carry Adders (RCA) are slower than Carry Look-Ahead Adders, especially as the number of bits increases.

[10] (CO4/K2)

06. Design a positive edge-triggered synchronous counter using T flip-flops for the sequence 0 → 1 → 3 → 7 → 6 → 4. Ensure unused states reset to 0 on the next clock pulse, and provide the timing diagram.

[10] (CO4/K4)

Section - III

Answer all Questions (4 × 15 Marks)

07. Design a digital logic system and realize the functions X, Y, and Z using logic gates for the bank security system represented in Figure 1. The security systems are placed at the bank's main gate, the locker room gate, and the locker box. Each security system has four types of verification methods: Fingerprint (A), Password (B), Pattern (C), and Iris Recognition (D). The gates open based on the following conditions:

(i) Bank gate opens (X) – Any one of the inputs (Fingerprint, Password, Pattern, or Iris Recognition) must match.

(ii) The locker room gate opens (Y). Any two inputs must match (Fingerprint, password, pattern, or Iris Recognition).

(iii) Locker box opens (Z) – Any three of the inputs must match, and Iris Recognition must be one of them.

Input Variables: Fingerprint, Password, Pattern, and Iris Recognition.
Output Variables: Bank gate open, Locker room gate open, Locker box open.

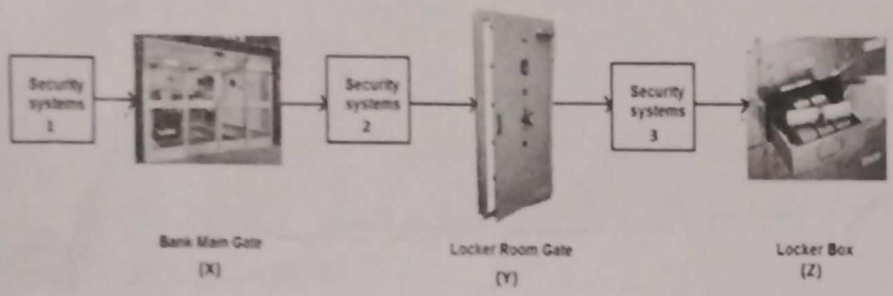

Figure 1

[15] (CO1/K3)

08. (a) Implement the full subtractor using two 1×4 demultiplexers. (7 Marks)
(b) The truth table of the priority encoder is given below. Compute the Boolean expressions for the outputs and draw the logic diagram. (8 Marks)

Input				Outputs		
D0	D1	D2	D3	x	y	v
1	X	X	X	1	1	1
0	1	X	X	1	0	1
0	0	1	X	0	1	1
0	0	0	1	0	0	1
0	0	0	0	X	X	0

[15] (CO3/K3)

09. Design a sequential circuit for a Moore-type FSM that produces an output 1 whenever the input sequence 10110 is detected. Use D flip-flop for the realization. (Note: overlapping sequences are accepted).

[15] (CO5/K4)

10. (a) Design a Programmable logic array system to implement a "one's count" circuit that works as follows. The subsystem has four inputs (A, B, C, and D) and generates a 3-bit output (XYZ). (10 Marks)

- XYZ = 000 → if none of the inputs are 1.
- XYZ = 001 → if one input is 1.
- XYZ = 010 → if two inputs are 1.
- XYZ = 011 → if three inputs are 1.
- XYZ = 100 → if all four inputs are 1

(b) What does FPGA stand for? List the advantages of FPGA over conventional processors. Also, give the role of LUT in FPGA. (5 Marks)

[15] (CO6/K3)

BL-Bloom's Taxonomy Levels - (K1-Remembering,K2-Understanding,K3-Applying,K4-Analysing,K5-Evaluating,K6-Creating)

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