Continuous Assessment Test (CAT) – I - AUGUST 2025

Programme	:	**B. Tech (ECE)**	Semester	:	**FALL 2025-26**
Course Code & Course Title	:	**BECE102L-DIGITAL SYSTEMS DESIGN**	Class Number	:	**CH2025260100390, CH2025260100392, CH2025260100394, CH2025260100395**
Faculty	:	**Dr. Sakthivel.SM, Dr B Lakshmi Dr. K Srivatsan, Dr. Gargi Raina**	Slot	:	**D1 + TD1**
Duration	:	**90 Minutes**	Max. Marks	:	**50**

General Instructions:

- Write only your registration number on the question paper in the box provided and do not write other information.
- Only non-programmable calculator without storage is permitted

Answer all questions

Q. No	Sub Sec.	Description	Marks	CO	Blooms Taxonomy Level
1.		i) Simplify the expression given below using Boolean theorems. $F = (X + Y + Z)(X'Y + Y'Z)$	**5**	**1**	**L3**
		ii) Draw the CMOS transistor-based network to implement given Boolean logic function. $F = [((AB + (C+D)).(EF)]$	**5**		**L3**
2.		Design the logic for an automatic gate controller that controls the gate for the following conditions • **A**: RFID tag detected • **B**: Face recognized • **C**: Gate is unlocked • **D**: Admin override is ON A gate opens (Z = 1) for the following situations: 1. If either RFID tag is detected or face is recognised along with the gate being unlocked 2. If the gate is locked, the gate will never open unless admin override is high 3. Irrespective of other inputs, admin override should always be high i) Construct the truth table for the above scenario. [4 Marks] ii) Derive the minimized Boolean expression using K-Map. [4 Marks]	**15**	**1**	**L4**

		iii) Implement the minimized boolean expression using basic logic gates. [3 Marks] iv) Implement the same logic using only NAND gates. [4 Marks]			
3.	(a)	Write a Verilog program that takes two 8-bit binary inputs, A and B, and performs the following operations: (i) compare whether A and B are equal, (ii) compute the bitwise OR of A and B, (iii) perform a NOR reduction on A, (iv) apply a logical right shift on B by 2 bits, and (v) create a 16-bit vector by repeating the bit pattern of A twice consecutively. Declare A and B as input ports, and store the results of each operation using appropriate Verilog constructs such as reg, wire or output, depending on the context of use. Ensure all operations are implemented using continuous or procedural assignments.	5	2	L1
	(b)	Draw the logic diagram for the Verilog HDL code provided below: *module prob_1 (T, X2, X3, W, f, g, h);* *input T, X2, X3, W;* *output reg f, g, h;* *always @(*)* *begin* *f = (T & ~X3) | (X2 & ~W);* *g = (~T & X3) | X2;* *h = (X2 & T) & W;* *end* *endmodule*	5		L2
4.	(a)	Implement the following function using a 1:2 decoder and two 3:8 decoders with enable $F(A.B,C,D) = A\bar{B}D + A\bar{B}\bar{C} + ADC + CD$	10	3	L3
	(b)	Write a verilog code in behavioral modelling for 2:4 decoder.	5		L2

**********All the best **********