VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Reg. Number:

# Continuous Assessment Test (CAT) – II - April 2024

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| Programme | : | B.Tech CSE & B.Tech CSE all Specializations | Semester | : | Winter Sem 23-24 |
| Course Code & Course Title | : | BCSE205L/CSE2001 and Computer Architecture and Organization | Class Number | : | CH2023240501631/ CH2023240501635/ CH2023240501642/ CH2023240503352/ CH2023240502851 |
| Faculty | : | Dr.Monica/ Dr.Vaidehi/Prof.Nivedita/ Dr.Thanikachalam | Slot | : | F1+TF1 |
| Duration | : | 90 Minutes | Max. Mark | | 50 Marks |

**Answer all questions**

| Q. No | Sub Sec. | Description | Marks |
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| 1. | | Illustrate the architectural design of a Single cycle data path to fetch and execute the following instructions. Write down the micro routine control sequence steps involved in the architecture with respect to the given instructions. (A, B, D are memory locations).<br><br>LOAD R1,A<br>DIV (R1),B<br>STORE R1,D | 10 |
| 2. | | Consider two processors (P1 and P2) executing a particular algorithm. The instructions can be divided into four classes along with their frequencies and Cycles Per Instruction given in the table below. P1 has a clock rate of 3 GHz and P2 with a clock rate of 2.5 GHz. Illustrate which implementation is faster? [5 marks]<br>Frequency CPI of P1 CPI of P2<br>Load 20 1 1<br>Store 30 2 3<br>Move 30 2 2<br>Jump 20 1 3 | 10 |
| | | Find the number of RAM Chips, address bits, and decoder size required to design a new RAM chip of size 1024 x 8 with the basic RAM chip of size 128 x 8. Explain the newly designed RAM Chip with a neat sketch. [5 marks] | |
| 3. | | Consider a 4-way set associative cache with a total of 12 cache blocks. The main memory block requests are as follows:<br><br>10, 55, 11, 4, 13, 8, 132, 129, 212, 129, 64, 8, 48, 32, 73, 92 | 10 |

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| | | Calculate the number of misses and the miss ratio if the replacement strategy is<br>i. Least Recently Used (LRU) [5 marks]<br>ii. First In First Out(FIFO)[5 marks] | |
| 4. | | Suppose that the processor has access to four levels of cache memory and Main Memory. Level 1 contains 100 words and has an access time of 0.1 microseconds; level 2 contains 1000 words and has an access time of 1 microsecond; level 3 contains 10000 words and has an access time of 2 microsecond ; level 4 contains 100000 words and has an access time of 3 microsecond. The access time for Main Memory is 10 microsecond. Suppose 50% of the memory accesses are found in level 1 cache, 30% in level 2, 10% in level 3 and 5% in level 4. Calculate the average time to access a word? | 10 |
| 5. | | The message $x^9+x^8+x^6+x^4+x^3+x+1$ needs to be transmitted using a code that has a generator polynomial $x^3 + x + 1$. Find the actual bit string that is transmitted. Using the same polynomial divisor and illustrate the receiver side verification. | 10 |