VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Reg. Number:	

Continuous Assessment Test(CAT) – II - April 2024

Programme	:	B.TECH	Semester	:	WIN 2023-24
Course Code & Course Title	:	BCSE205L- Computer Architecture and Organization	Class Number	:	CH2023240502012 CH2023240502018 CH2023240502008
Faculty	:	Prof. NIVEDITA M Dr. A. K ILAVARASI Dr. S. PAVITHRA	Slot	:	C1+TC1
Duration	:	90 Mins	Max. Mark		50

General Instructions: < Use this space to provide additional information such as graph sheet, data book etc.>

- Write only your registration number on the question paper in the box provided and do not write other information.
- Use statistical tables supplied from the exam cell as necessary
- Use graph sheets supplied from the exam cell as necessary
- Only non-programmable calculator without storage is permitted

Answer all questions

Q. No	Sub Sec.	Description	Marks
1	a	Consider a multicycle bus organization to execute the set of instructions: *Move #20, R3* *Mul (R2), R3, R4,* Where, Register R2 holds the address of the source operand 1 and source operand 2 resides at Register R3. The result is stored in Register R4. Draw the multicycle data path and Write the control sequence to fetch and execute the given instructions.(10 marks)	15
	b	Consider the execution of a program which has 1 million instructions that is run on a 200 MHZ processor. The CPI for each instruction type and the proportion of each type of instructions is given below.	

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load/Store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

Calculate the MIPS rate. (5 marks)

2		A computer has to be interfaced with a memory module that consists of a 2M x 32 RAM. i. How will the address bits be decoded for each memory module of this organization? (4 marks) ii. Construct this memory module using 512K x 8 RAM chips. Discuss with appropriate diagram. (6 marks)	10
3		Consider a cache with 128 blocks and a block size of 16 bytes. For the given configuration, identify the block number to which the block 1200 would map if the following mapping schemes were used. a. Direct mapping b. 2-way set associative mapping	5
4		Given a 4-way set associative cache with a capacity of 16 words and each block has 1 word .Consider the blocks requested by the processor: 1,5,9,4,22,18,8,19,58,9,11,48,4,16,43,5,6,9,21,17,34,20,8,40. Calculate the Hit ratio, miss rate and final contents of the cache when LRU replacement strategy is used.	10
5		i. The data transmitted is $(11010000)_2$ and the syndrome word is $(0011)_2$. Find the odd parity check bits at the receiver side using Hamming Code Procedure. How is the error correction performed? (5 marks) ii. The data transmitted over a communication channel is $(111111100)_2$ and the polynomial expression corresponding to the divisor is x^2+x+1. The Received data is corrupted by 1 bit $(111111000)_2$. Apply the Cyclic Redundancy Check (CRC) method to find that there is data error in the transmission. (5 marks)	10
********** All the best **********			