VIT
Vellore Institute of Technology

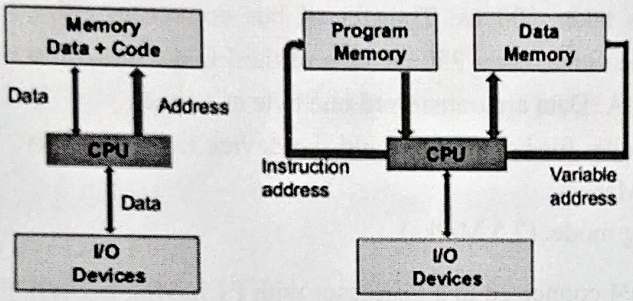
Reg. No. :

Final Assessment Test (FAT) - November/December 2023

Programme	**B.Tech.**	Semester	**FALL SEMESTER 2023 - 24**
Course Title	**COMPUTER ARCHITECTURE AND ORGANIZATION**	Course Code	**BCSE205L**
Faculty Name	**Prof. PAVITHRA S**	Slot	**G1+TG1**
		Class Nbr	**CH2023240100673**
Time	**3 Hours**	Max. Marks	**100**

PART - A (7 X 10 Marks)
Answer all questions

01. Consider the below two architectures A and B. **[10]**



A B

BEGIN
NUMBER counter, sum=0
FOR counter=1 TO 100 STEP 1 DO
sum=sum+counter
END FOR
OUTPUT sum
END

a) How will the pseudo code given be executed in systems A and B? [5 Marks]

b) Discuss the step by step execution of the given pseudo code on the two systems in detail. [5 Marks]

02. Prove that multiplication of two n-digit signed numbers in base 2 gives a product of no more than 2n digits with $(-20)_{10}$* $(+15)_{10}$. **[10]**

03. a) Illustrate the complete control sequence of the Single Cycle Data Path and Multiple Cycle Data path to fetch and execute the instruction: MUL R1, (R2), R3. (Assume R2 and R3 as source and R1 as destination). The instructions should show the steps of fetch and execute phases. (7 Marks) **[10]**

b) Show the pros and cons of the single-bus organization over the multi-bus. (3 Marks)

04. Compare the performance of two different computers: M1 and M2. The following measurements have been made on these computers: **[10]**

a) Which computer is faster in terms of execution time for each program and by what ratio? (3 Marks)

b) Find the instruction execution rate (instructions per second) for each computer while executing program 1. (3 Marks)

c) The clock rates for M1 and M2 are 3 GHz and 5 GHz respectively. Find the CPI for program 1 on both machines. (4 Marks)

05. A cache has 64KB capacity; 128 byte lines and is 4-way set associative. The system containing cache has 32-bit address.[2.5 Marks each] [10]

a) How many bits of tag are required in each entry in the tag array?

b) Find the tag directory size.

c) If the cache is write-through, how many bits are required for each entry in the tag array and how much storage is required for the tag array if an LRU replacement policy is used?

d) If the cache is write-back, how many bits are required for each entry in the tag array?

06. a) Identify the data transfer technique used for writing a byte data from the processor to a peripheral device which is not controlled by a common clock pulse and explain its functionality using appropriate timing diagrams. (5 Marks) [10]

b) Consider a system in which bus cycles takes 500 ns. Transfer of bus control in either direction, from processor to I/O device or vice versa, takes 250 ns. One of the I/O devices has a data transfer rate of 50 KB/s and employs DMA. Data are transferred one byte at a time.

i. Suppose we employ DMA in burst mode, for how long would the device tie up the bus when transferring a block of 128 bytes? (2.5 Marks)

ii. Repeat the calculation for cycle-stealing mode. (2.5 Marks)

07. Consider four peripheral devices P1, P2, P3, P4 connected to a Processor with P1 having highest priority and P4 having lowest priority. Analyze the following bus arbitration methods with respect to communication reliability in the event of P1 failure. [10]

a) Daisy Chaining (4 Marks)

b) Polling (3 Marks)

c) Independent Request (3 Marks)

PART - B (2 X 15 Marks)

Answer all questions

08. a) Consider a 4-drive, 200GB per drive RAID array. What is the available data storage capacity for each of the RAID levels 0, 1, 3, 4, 5 and 6? Justify your answer. (10 Marks) [15]

b) A manufacturer wishes to design an array of hard disks in a server with a capacity of 512 GB or more. If the technology used to manufacture the disk allows 2048-byte sectors, 4096 sectors/track and 8192 tracks/platter, how many disks are required, assuming two platters/disk? (5 Marks)

09. a) Identify and explain the dependencies in the following code when executed in a 5-stage pipelined processor. How will you resolve the dependencies? Sketch the pipelining stages and identify the stall(s) if any. (10 Marks) [15]

```
add R3, R4, R2
sub R5, R3, R1
load R6, 200(R3)
add R7, R3, R6
```

Note: In the above instruction format, first operand is the destination and other operands are source operands.

b) Given the following code snippet, Identify the suitable Flynn's Taxonomy classification and explain it. (5 Marks)

```
for ( i = 0; i < n; i++)
 for ( j = 0; j < n; j++)
  for( k = 0; k < n; k++)
   C[i,j] = C[i,j] + A[i,k] * B[k,j]
  end for
 end for
end for
```