Reg. No.:

Name :

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test I – January- 2025

Programme	: B.Tech (ECE/ECM/VLSI/CSE)		Semester	:	WS 2024-25
Course	: DIGITAL SYSTEM DESIGN		Code	:	BECE102L
			Class Nbr	:	CH2024250501924
Faculty	: Dr.MANMOHAN SHARMA		Slot	:	B1+TB1
Time	: 90 Minutes		Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks	BT Level
1.		(a)Design a combinational circuit with three inputs and one output, for the condition: The output is 1 when the binary value of the inputs is less than or equal to 3. The output is 0 otherwise. (5 marks) (b)Use POS K-Map to obtain the minimum literal Boolean expression and draw the NOR only schematic for the same. (5 marks)	10	1
2.		Design the static CMOS Logic circuit for the expression F= (A + (B' + CD)')'.	5	1
3.		A smart sprinkler automatically waters the plants based on the Season, soil conditions such as Season (S=1 if Summer; else=0), Moisture content of the soil (M=1 if High; 0 if low), Temperature (T=1 if High; 0 if low), and Humidity (H=1 if High, 0 if low). The sprinkler will turn "ON" if any of the conditions are met: (i) Moisture content is low in winter. (ii) Temperature is high and Moisture content is low in Summer. (iii) Temperature is high and Humidity is High in Summer. (iv) Temperature is low and Moisture content is low in Summer. (v) Temperature is high and Humidity is low. (a)Obtain the truth table by using the above conditions and write the expression in terms of minterms and maxterms. Sketch the K-Map in SOP and POS form. (8 marks) (b) Obtain their minimal expression and draw the logic diagram in SOP form. (7 marks)	15	3
4.	(I)	Determine the value of "result" in each of the following instructions. [3 × 2 = 6 Marks] (a) **regA = 4'b1101; regB = 4'b0110;** **result = (&regA) + (|regB) + (^regA);** (b) **regA = 6'b110; regB = 6'd10;** **result = ((regA + regB) << 2) - regB;** (c) **regA = 5'b1010; regB = 5'b0101;** **result = (regA ^ regB) + {3'b0,1'b1};**	6	4
	(II)	A digital logic circuit is operated as specified in the following truth table. Express the SOP expression for the output of the digital circuit and write the Verilog Source code	4	4

that implements the same using gate level modelling style.

Inputs			Output
C	A	B	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

5. (I) Design a half subtractor using NOR gate. Design should include truth table, expression and logic diagram 5 1

(II) Write the Verilog HDL description for the circuit which adds two binary bits along with carry in data flow modelling. Also, write the testbench for the same. 5 4

⇔⇔⇔