VIT
Vellore Institute of Technology
CHENNAI

Reg. Number: 24BAI1588

Continuous Assessment Test (CAT) – I -JAN 2025

Programme	:	B.Tech(CSE,EEE)	Semester	:	FS 2024-25
Course Code & Course Title	:	BECE102L & Digital System Design	Class Number	:	CH2024250501659, CH2024250501667, CH2024250501674, CH2024250501682, CH2024250501691, CH2024250501700, CH2024250501711, CH2024250501719, CH2024250501753 CH2024250501624, CH2024250501638
Faculty	:	Dr. Gargi Raina, Dr. Subhashini. N, Dr. Sasithradevi. A, Dr. P. Nirmala, Dr. Sourabh Paul, Dr. Srivatsan. K, Dr. Girija Sankar, Dr. Sukriti, Dr. Sathya Sree, Dr. Sriramalakshmi. P, Dr. Vimala Gayathri.	Slot	:	A1+TA1
Duration	:	90 Minutes	Max. Mark		50

General Instructions:

- Write only your registration number on the question paper in the box provided and do not write other information.

Answer all questions

Q. No	Sub Sec.	Description	Marks	Blooms Taxonomy Level
1		i. Reduce the Boolean expression $G = A'B(D' + C'D) + B(A + A'CD)$ to minimum number of literals. ii. Find the complement of the function $F = WX + YZ$ by applying De-Morgan's theorem. Also find $F.F'$ iii. Draw the logic diagram of the function $H = BC' + AB + ACD$ iv. Write the function H in canonical Sum of Products.	10 [2+3+ 2+3]	L3
2		Design a combinational logic circuit used to instruct a Floor cleaning robot to recharge (R=1) itself only when a specific set of following conditions is met. (i). When its battery is low (B = 1) or (ii). When the working time is over (T=1) or (iii). When vacuuming is complete (V=1), and when waxing is complete (W=1). (a) Construct a truth table for floor cleaning robot to recharge. (b) Obtain the simplified Boolean expression using K-map. (c) Construct Logical circuit for the obtained simplified Boolean expression using only NAND gate.	10	L4
3		Implement the function $F = \overline{(A + B + C).(D.E)}$ using static CMOS logic style.	5	L1

4		For the Verilog HDL code given, assume if the inputs are A=4'b1100, B=4'b1001 C=4'b1010, D=4'b1110, E=2'b10 compute their output F, P, Q, R, S. Show necessary steps involved in computing final output values.
		module test_logic(F,P,Q,R,S,A,B,C,D,E);
		input [3:0]A,B,C,D;
		input [1:0]E;
		output [3:0]F,P,R;
		output [7:0]Q;
		output S;
		reg [3:0]F,P,R;
		reg [7:0]Q;
		reg S;
		always @(A,B,C,D,E)
		begin
		F=~(A^B);
		P= D << 3;
		Q={{2{E}},C};
		R=B>>3;
		S=(C!==D);
		end
		endmodule
			5	L3

5		Identify the five errors present in the Verilog HDL code of a full adder, which is implemented by instantiating a half adder module twice.
		
		module 2FA(a,b,cin,sum,cout);
		input a,b,cin;
		output sum,cout;
		wire x,y,z;
		HA h1(a,b,x,y);
		ha h2(sum,z,x,cin);
		or(couT,y,z);
		endmodule;
		
		module ha(a,b,sum,cout);
		input a,b;
		output sum,cout;
		xor(sum,a,b);
		and(cout,a,b);
		endmodule
			5	L3

6		A decoder, combined with an OR gate connected to its output terminals, can be utilized for synthesizing combinational networks. i. Implement the function F using suitable decoder. $F(A,B,C,D) = A'B'D + A'BD + AC'D' + ACD'$ ii. Write the Verilog HDL code for the design described in part (i)	15 [8+7]	L2,L4
		Total Marks	50	