Reg. No.:

Name :

VIT®

Vellore Institute of Technology

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Continuous Assessment Test II – March- 2025

Programme	: **B.Tech (ECE/ECM/VLSI/CSE)**	Semester	:	**WS 2024-25**
Course	: **DIGITAL SYSTEM DESIGN**	Code	:	**BECE102L**
		Class Nbr	:	**CH2024250501924**
Faculty	: **Manmohan Sharma**	Slot	:	**B1+TB1**
Time	: **90 Minutes**	Max. Marks	:	**50**

Answer All the Questions

Q.No.	Sub. Sec.	Questions	Marks	BT Lvel
1		Implement the Boolean function $F(A,B,C,D)=\sum_m(1,3,4,6,7,9,12,13)$ using a. 8×1 Multiplexer with A, C, and D as selection lines. **[4 Marks]** b. 4×1 Multiplexer with B and C as selection lines. **[6 Marks]**	10	3
2	a	The two bulbs (B1, B2) in a staircase have four switches (S1, S2, S3, S4), one switch being on the ground floor, remaining are placed on the 3rd floor. The B1 can be turned ON when **S1=S4** but **S2 is not equal to S3** but **B2** can be turned ON by **S1=S3 and S2=S4** and in other cases, B1 and B2 are on OFF state. Implement the logic using the appropriate Decoder circuit. **[6 Marks].**	10	2
	b	Write a Verilog program to implement the same using structural modeling. **[4 Marks]**		
3		Write a Verilog program using the behavioral modeling approach to implement a 4-bit magnitude comparator. The module should compare two 4-bit binary numbers and determine whether one is greater than, less than, or equal to the other.	5	2
4		Perform multiplication of (-12) x (+8) using Booth's Multiplication algorithm. Also list out the number of additions, number of subtractions and number of arithmetic shifts required.	10	3
5		Convert a two input sequential circuit that has forbidden state into single input sequential circuit that toggles when the input is high.	4	3
6		Sketch the Q output waveform for both the D- latch and D-FF for the clock and data inputs shown below	4	2

7		Derive the state table for the circuit shown in Figure. Assume the top flip flop is in LSB position and bottom is in MSB position.	7	2