VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test – 1, August 2024

Programme	:	**B. Tech. CSE**	Semester	:	**Fall 2024 - '25**
Course	:	**Basic Electrical and Electronics Engineering**	Code	:	**BEEE102L**
Faculty	:	**D. R. Binu Ben Jose**	Slot	:	**C1+TC1**
		Common question across C1 slot	Class Number	:	**CH2024250103732**
Time	:	**$1\frac{1}{2}$ Hours**	Max. Marks	:	**50**

Answer ALL the Questions (5 x 10 = 50 Marks)

1. Use mesh analysis to find V_o marked in the circuit shown in Fig. 1. **(10)**

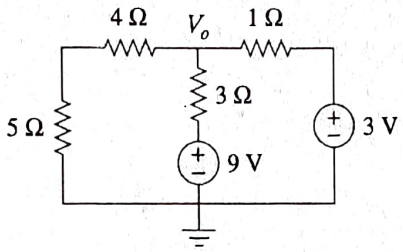

Fig. 1

2. Find the voltages v_1 **and** v_2 marked in the circuit shown in Fig. 2 using nodal analysis. **(10)**

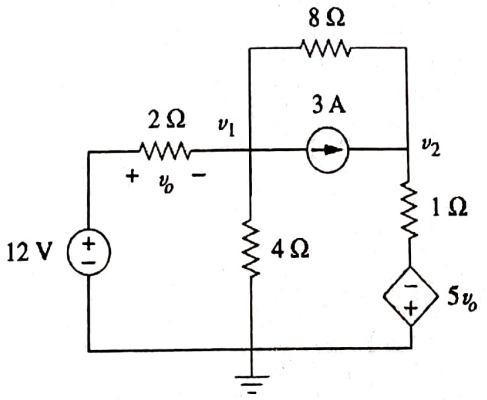

Fig. 2

3. Compute the **current** i marked in the circuit shown in Fig. 3 using Superposition principle. **(10)**

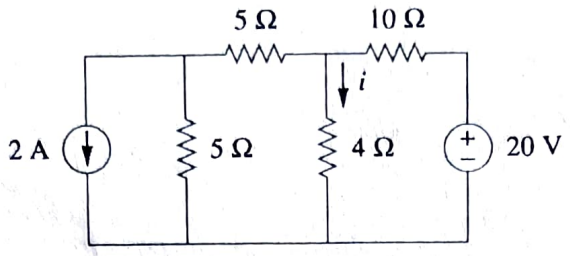

Fig. 3

4. In the circuit in Fig. 4, a load resistance of value **10 Ω** is connected across the terminals **a-b**.
   (a) For what value of load resistance will the maximum power be delivered to the load? **(4)**
   (b) Compute the maximum power that can be delivered by the circuit. **(6)**

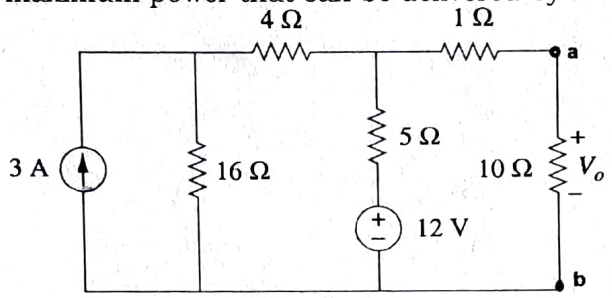

Fig. 4

5. A load impedance Z is connected across a voltage source

$$v(t) = 12\,sin\,(10t + 20^o)\,V\,.$$

   (a) If the current drawn by the load is $i(t) = 5\,cos\,(10t - 30^o)\,A$, find the phase angle between voltage and current. Comment on whether the current leads or lags the voltage. **(4)**

   (b) If the load consists of a resistor **R = 5 Ω**, an inductor **L = 0.2 H** and a capacitor **C = 0.1 F** are connected in series, compute the current drawn by the load. **(6)**

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