VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Reg. Number:	

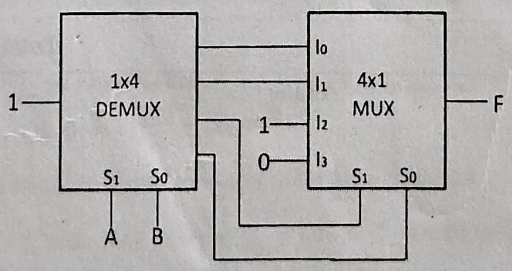
Continuous Assessment Test (CAT) –II- March 2025

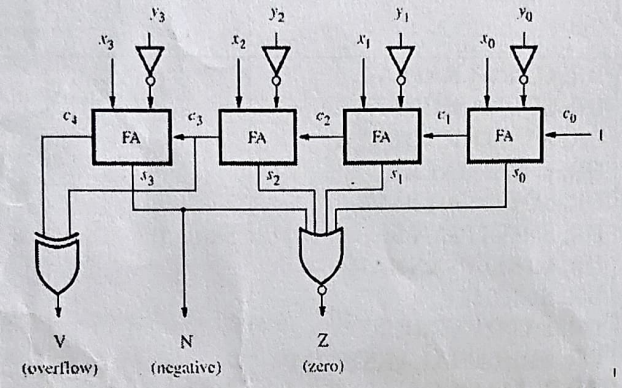
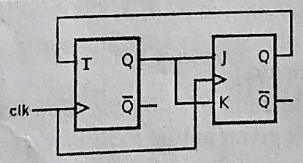
Programme	:	**B.Tech (CSE/EEE)**	Semester	:	**WS 2024-25**
Course Code & Course Title	:	**BECE102L & Digital Systems Design**	Class Number	:	**CH2024250501659, CH2024250501667, CH2024250501674, CH2024250501682, CH2024250501691, CH2024250501700, CH2024250501711, CH2024250501719, CH2024250501753 CH2024250501624, CH2024250501638**
Faculty	:	**DR. GARGI RAINA DR. SUBHASHINI N DR. SASITHRADEVI A DR. P. NIRMALA DR. SOURABH PAUL DR. SRIVATSAN K DR. GIRIJA SANKAR DR. SUKRITI DR. SATHYA SREE DR. SRIRAMALAKSHMI P DR. VIMALA GAYATHRI**	Slot	:	**A1+TA1**
Duration	:	**90 minutes**	Max. Mark		**50**

General Instructions:

- Write only your registration number on the question paper in the box provided and do not write other information.
- Only non-programmable calculator without storage is permitted.

Answer all questions

Q. No	Sub Sec.	Description	Marks	BT Level
1.		**(i)** Implement the logic function $F(A,B,C,D) = AC + ABD + ACD$ using only one 4×1 multiplexer and external gate(s). [7 marks] **(ii)** Find the Boolean function $F(A,B)$ for the following combinational circuit given in Fig. 1. [8 marks]  **Fig. 1.**	15	L3

2.		In an industrial automation system, 4-bit sensor readings are sent to a remote processing unit. To ensure reliability, an additional bit is appended to each transmission, making sure the total count of 1s remains odd. Identify the circuit responsible for generating this extra bit. Represent its truth table, logical expression and draw the circuit diagram.	5	L2
3.		Perform multiplication of **-19** & **07** using Booth's multiplication algorithm with its stepwise operations.	10	L2
4.		Identify and explain the circuit shown in Fig. 2. Write a structural Verilog code that describes the behaviour of the given circuit, establishing the relationship between the inputs ($x_3x_2x_1x_0$, $y_3y_2y_1y_0$, and c_0) and the outputs ($s_3s_2s_1s_0$, c_4, V, N, and Z).  **Fig. 2.**	10	L3
5.		For the logic diagram shown in below Fig. 3, assume that the T flip-flop initially has a HIGH output, while the JK flip-flop starts with a LOW output. Formulate a table as shown below representing the sequence of outputs produced from J-K flip flop for the next 5 clock pulses. clk | T | Q_T | Q_{T+1} | J | K | Q_{JK} | Q_{JK+1}  **Fig. 3.**	10	L3
		Total	**50**	

**********All the best **********